AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-10. (Cancelled)

11. (Currently Amended) A semiconductor integrated circuit device which has a signal input point, a signal output point, and plural circuit blocks provided in series between the signal input point and the signal output point and in which the timings of a signal input operation from the signal input point, a signal output operation at the signal output point, and a signal transmission operation among the plural circuit blocks are respectively controlled by timing signals,

wherein each said circuit block has plural latches and an individual signal response period between a timing when a first latch of the circuit block fetches a signal and a timing when the circuit block outputs a signal that is fetched by a first latch of the next circuit block, and

wherein, when the clock signal cycle is T1, ~~the~~ a total of the signal response periods ~~of the plural circuit blocks~~

~~is T2, and the ratio T2/T1 between T1 and T2 is n+α (n is an integer and α is a positive number equal to or less than 1), a signal response period~~ from the signal input point to the signal output point is ~~set to n+1 times~~ adjusted from a non-integer multiple to an integer multiple of the clock signal cycle T1.

12-19. (Cancelled)

20. (Original) The semiconductor integrated circuit device according to Claim 11,

wherein said plural circuit blocks include a first circuit block and a second circuit block,

wherein said first circuit block receives a signal input in accordance with a first timing signal,

wherein said second circuit block outputs a signal output in accordance with a second timing signal,

wherein said first and second timing signals are controlled by said clock signal.

21. (Original) The semiconductor integrated circuit device according to Claim 20, further comprising:

a timing generating circuit which generates said first and second timing signals in accordance with said clock signal;

a plurality of DRAM macro cells;

a read and write buffer; and

an address decoder,

wherein said timing generating circuit includes a delay circuit which is programmable.

22. (Previously Presented) The semiconductor integrated circuit device according to Claim 21,

wherein a time difference between said first and second timing signals is other than a multiple cycle of said clock signal.

23. (Original) The semiconductor integrated circuit device according to Claim 21, further comprising:

a redundancy address setting circuit including fuses, and

wherein said timing generating circuit includes fuses.